AMENDMENTS TO THE CLAIMS

Please cancel claims 2 and 30 without prejudice and amend Claims 1, 16 and 29 as follows:

1. (*Currently amended*) N integrated transformers comprising:

a plurality of conducting stripes formed closely to each other in silicon, each two adjacent stripes of the conducting stripes forming one of the N transformers;

a grounding stripe deposited between two adjacent transforms of the N transformers to shield cross-coupling between the two adjacent transforms; and

wherein none of the conducting stripes are electrically connected and N is a finite integer greater than or equal to 2.

2. (*Cancelled*)

3. (*Original*) The transformers as recited in claim 1, wherein the conducting stripes are on a layer and wound in parallel into a flat spiral that has a shape in accordance with a predefined area in silicon for the transformers.

4. (*Original*) The transformers as recited in claim 1, wherein the conducting stripes are transmission lines on a layer and wound in parallel in an available area.

5. (*Original*) The transformers as recited in claim 1, wherein a first set of the conducting stripes are on a layer and wound in parallel into a flat spiral that has a shape in accordance with a predefined area in silicon for the transformers, and a second set of the conducting stripes are on the same layer and wound in parallel into the same flat spiral but in opposite direction to the first set.

6. (Withdrawn) The transformers as recited in claim 5, wherein the first set and the second set of the conducting stripes are interlaced with each other.

7. (*Original*) The transformers as recited in claim 5, wherein the conducting stripes are respectively extended to one or more layers to increase conductance of each of the conducting stripes, the one or more layers are within a silicon space.

8. (*Original*) The transformers as recited in claim 1, wherein the conducting stripes are extended to one or more layers for increased inductance in each of the conducting stripes.

9. (Withdrawn) The transformers as recited in claim 8, wherein the extended portions of the conducting stripes on the one or more layers being arranged in a similar fashion as those of the conducting stripes on a first layer.

10. (Withdrawn) The transformers as recited in claim 9, wherein the one or more layers are stacked on top of each other, one or more grounding walls are formed across the layers to minimize cross-coupling between or among the layers.

11. (Withdrawn) The transformers as recited in claim 1, wherein a first half of the conducting stripes are in a first layer and a second half of the conducting stripes are in a second layer, and wherein the first layer and the second layer are arranged on top of each other such that the first half of the conducting stripes correspond to the second half of the conducting stripes to form the N integrated transformers.

12. (Withdrawn) The transformers as recited in claim 11, wherein there is a grounding stripe to separate one conducting stripe from another in the first layer and the second layer to shield any possible cross-coupling among the N integrated transformers.

13. (Withdrawn) The transformers as recited in claim 11, wherein the first half of the conducting stripes are extended to a first set of one or more layers for increased inductance in each of first half of the conducting stripes, the second half of the conducting stripes are extended to a second set of one or more layers for increased inductance in each of second half of the conducting stripes, and wherein the first and

second set of one or more layers are stacked or interlaced on top on each other to form a pair of two layers to extend the transformers formed on the first two layers.

14. (Withdrawn) The transformers as recited in claim 13, wherein a grounding stripe is formed between every two of the conducting stripes to minimize cross-coupling among the transformers.

15. (Withdrawn) The transformers as recited in claim 13, wherein a grounding wall is formed across the layers to minimize cross-coupling among the layers.

16. (*Currently amended*) The transformers as recited in claim 1, wherein the conducting stripes are communication lines extended to a plurality of several layers that are stacked on top of each other without any insulating layers in between to increase magnetic coupling between the layers.

17. (Withdrawn) The transformers as recited in claim 1, wherein at least one of the N transformers are surrounded by many others of the N transformers on a layer.

18. (*Original*) The transformers as recited in claim 1, wherein the N integrated transformers are employed in an allocated silicon space for an integrated circuit.

19. (*Original*) The transformers as recited in claim 18, wherein the N integrated transformers are used to replace N similar transformers that would otherwise occupy multiple silicon spaces for the N similar transformers.

20. (*Original*) The transformers as recited in claim 18, wherein each of the N integrated transformers is employed in a differential circuit in the integrated circuit, together with parasitic effects of transistors in the differential circuit, to provide resonant filtering to minimize artifacts or distortions in signals processed in the differential circuit.

21. (*Withdrawn*) N integrated transformers comprising:

a first group of N conducting stripes formed in a first layer, the first group of the N conducting stripes wound into a first flat spiral on the first layer;

a second group of N conducting stripes formed in a second layer, the second group of the N conducting stripes wound into a second flat spiral on the second layer,

wherein the first flat spiral and the second flat spiral are substantially identical so that the first group of the N conducting stripes correspond to the second group of the N conducting stripes when the first layer and the second layer are on top of each other, and

wherein none of the conducting stripes are electrically connected and N is a finite integer greater than or equal to 2.

22. (*Withdrawn*) The transformers as recited in claim 21, wherein a grounding stripe is deposited between every two of the N conducting stripes on the first layer and the second layer such that undesired cross-couplings between or among some of the N conducting stripes on the first layer and the second layer are minimized.

23. (*Withdrawn*) The transformers as recited in claim 22, wherein the first group and the second group of the N conducting stripes are continuously extended to one or more layers to increase inductance of each of the N conducting stripes.

24. (*Withdrawn*) The transformers as recited in claim 23, wherein the extended portions of the N conducting stripes are also wound in similar fashion to that in the first and/or second layer.

25. (*Withdrawn*) The transformers as recited in claim 24, wherein, when the first, the second and the one or more layers are stacked, each of the transformers has increased inductance and coupling factor.

26. (*Withdrawn*) The transformers as recited in claim 25, wherein a grounding wall is formed across the layers to minimize undesirable cross-coupling between or among the layers.

27. (*Withdrawn*) The transformers as recited in claim 26, wherein the grounding wall is formed by a through-wafer via technology process.

28. (*Withdrawn*) The transformers as recited in claim 21, wherein a grounding stripe is formed between each two of the N conducting stripes are transmission lines on a layer and wound in parallel in an available area around a circuit.

29. (*Withdrawn - Currently amended*) A method for forming N integrated transformers, the method comprising:

forming a plurality of conducting stripes closely to each other in silicon, each two adjacent stripes of the conducting stripes forming one of the N transformers when signals with frequencies pass through the N transformers;

depositing a grounding stripe between two adjacent transforms of the N transformers to shield cross-coupling between the two adjacent transforms; and

wherein none of the conducting stripes are electrically connected and N is a finite integer greater than or equal to 2.

30. (*Cancelled*)

31. (*Withdrawn*) The method as recited in claim 29, wherein the conducting stripes are on a layer and wound in parallel into a flat spiral that has a shape in accordance with a predefined area in silicon for the transformers.

32. (*Withdrawn*) The method as recited in claim 29, wherein the conducting stripes are respectively extended to one or more layers to increase conductance of each of the conducting stripes, the one or more layers are within a silicon space.

33. (*Withdrawn*) The method as recited in claim 32, further comprising forming a grounding wall across the layers to shield cross-coupling between and among the layers.

34. (*Withdrawn*) The method as recited in claim 29, wherein a first set of the conducting stripes are on a layer and wound in parallel into a flat spiral that has a shape in accordance with a predefined area in silicon for the transformers, and a second set of the conducting stripes are on the same layer and wound in parallel into the same flat spiral but in opposite direction to the first set.

35. (*Withdrawn*) The method as recited in claim 34, wherein the first set and the second set of the conducting stripes are interlaced with each other.

36. (*Withdrawn*) The method as recited in claim 29, further comprising extending the conducting stripes to one or more layers for increased inductance in each of the conducting stripes.

37. (*Withdrawn*) The method as recited in claim 36, wherein the extended portions of the conducting stripes on the one or more layers being arranged in a similar fashion as those of the conducting stripes on a first layer.

38. (*Withdrawn*) The method as recited in claim 37, further comprising stacking the one or more layers in a silicon area.

39. (*Withdrawn*) The method as recited in claim 29, wherein a first half of the conducting stripes are in a first layer and a second half of the conducting stripes are in a second layer, and wherein the first layer and the second layer are arranged on top of each other such that the first half of the conducting stripes correspond to the second half of the conducting stripes to form the N integrated transformers.

40. (*Withdrawn*) The method as recited in claim 39, further comprising forming, placing or depositing a grounding stripe to separate one conducting stripe from another in the first layer and the second layer to shield any possible cross-coupling among the N integrated transformers.

41. (*Withdrawn*) The method as recited in claim 40, wherein the first half of the conducting stripes are extended to a first set of one or more layers for increased inductance in each of first half of the conducting stripes, the second half of the conducting stripes are extended to a second set of one or more layers for increased inductance in each of second half of the conducting stripes, and the method further comprising causing the first and second set of one or more layers to be stacked or interlaced on top of each other to form a pair of two layers to extend the transformers formed on the first two layers.

42. (*Withdrawn*) The method as recited in claim 41, the method further comprising forming, placing or depositing a grounding stripe between every two of the conducting stripes to minimize cross-coupling among the layers.

43. (*Withdrawn*) The method as recited in claim 39, further comprising forming a grounding wall across the layers to shield cross-coupling between or among the layers.

44. (*Withdrawn*) The method as recited in claim 29, wherein the conducting stripes are communication lines extended to a plurality of several layers that are stacked on top of each other.

45. (*Withdrawn*) The method as recited in claim 29, wherein the N integrated transformers are formed in an allocated silicon space for an integrated circuit including transistors and resistors.

46. (*Withdrawn*) The method as recited in claim 29, wherein each of the N integrated transformers is employed in a differential circuit in the integrated circuit, together with parasitic effects of transistors in the differential circuit, to provide resonant filtering to minimize artifacts or distortions in signals processed in the differential circuit.

47. (*Withdrawn*) The method as recited in claim 29, wherein at least one of the N transformers are surrounded by many others of the N transformers on a layer.